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August 21, 2007

VIA FACSIMILE
(Total No. of Pages Transmitted: 28)

To: Examiner Vicary
Group Art Unit No. 2183
Facsimile No.: (571) 273-8300/270-2314

From: Frederick E. Cooperrider
Facsimile No.: (703) 761-2375 or 76

Re: Slides for Telephone Interview
U.S. Patent Application Serial No. 10/671,889
Attorney Docket No. YOR.464

Examiner Vicary:

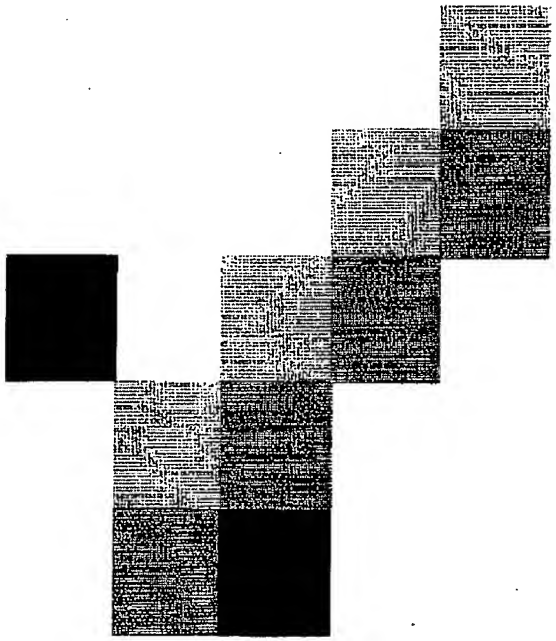
Enclosed are powerpoint slides to be discussed at today's telephone interview at 2:00. To join in the conference call, please dial 866-867-8308, then enter passcode 4192240 followed by # sign. If you have trouble joining the telephone interview, please call my office number at 703-761-4100.

Thank you in advance for your kind consideration on this case.

Very truly yours,

Frederick E. Cooperrider
Registration No. 36,769

FEC/fec
Enclosure



Patent Application 10/671,889 aka 170

Fred Gustavson

IBM Research

August 6, 2007

Overview of Talk

- Respond to OAS of 7/16/07
- 2 to 26(a. to d.): double patenting
  - preloading and pre-fetching are different
- 27-41(e. to j.) :112 rejections
- 42-46(k. to l.) :101 rejections
- 47-58:102 rejections

Overview of Talk continued

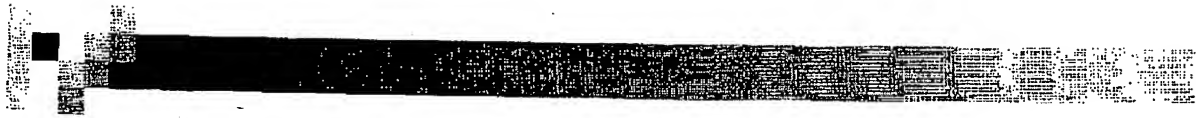
- 59 to 63: response to 6/17/07 arguments
- 64-66(m.) : Conclusions
  - new Gustavson reference of 1994 refers to L2 algorithmic pre-fetching
  - this patent refers to new forms of L3 pre-fetching

Overview of Talk continued

- Try to resolve issues before we produce a second Amendment (called A from now on)
  - can we resolve any rejected 101 claims?
  - can we resolve any rejected 112 claims?
  - can we resolve any rejected 102 claims?
  - can we resolve double patenting claim?

Attached Floating Point Units 1.

- L1 is not directly attached to L0
  - L0 is the register file of FPU
- data must arrive in L1 that is optimal for loading into L0
- pre-fetching get data to L1
- pre-loading get data to L0
- non-optimal and optimal cases for L1 to L0



Attached Floating Point Units 2

- multiple load instructions
  - quad loads done twice as fast as double loads
  - data for quad loads must be contiguous
- multiple loads not part of Gustavson 1998
- pre-fetching does no good unless quad loads can be used
- standard data structures cannot be used for multiple loads
- register blocking of co-pending patent ..888 is required for use of multiple loads

Attached Floating Point Units 3

- standard data structures requires 2NB + MB pre-fetch streams
  - typical values are NB=MB= 4 or 6
- some processors do not provide 12 or 18 pre-fetch hardware streams
  - IBM BG/L processor is an example
- with register blocking the number of such streams is 3 which is minimal for matrix multiply
- register blocking with minimum number of pre-fetch streams is not in Gustavson references

Double Patenting Issues 1.

- Even for some older machines without an attached FPU there was a distinction between pre-fetching and preloading
- We now concentrate only on newer machines since the Gustavson references
- consider using standard data structures so that data arrives in L1 that cannot use multiple loads

Double Patenting Issues 2.

- one must use multiple loads which will be incorrect for the application of matrix multiply
- some processors allow FPU register load instructions that can be overlapped with FPU multiple operations
  - this is a case where a new form of pre-loading can be utilized
- this new form of pre-loading is not covered in the Gustavson references

Items 2 to 26 discussions: 5. i

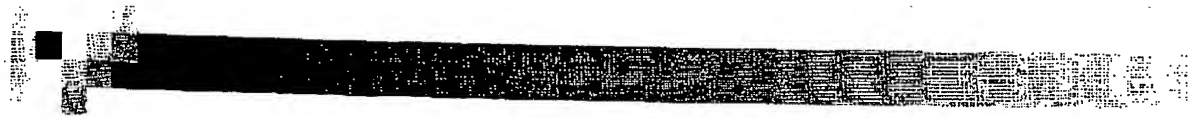
- Item 5: do you now see a distinction between pre-fetching & preloading?
  - pre-fetching gets data into L1
  - data may not be contiguous for multiple load instructions
  - must use multiple load instructions to get peak FPU performance

Items 2 to 26 discussions: 5. ii

- pre-loading uses overlapping load instructions of the FPU unit
  - different from multiple load instructions of the load store unit of a processor
  - incorrectly loaded data by multiple load instructions is corrected by using overlapping load instructions of the FPU unit
- above procedure is a new form of pre-loading not described in the Gustavson references

Items 2 to 26 discussions: 5. iii

- current 5 i, ii, slides are novel and not obvious to one skilled in the art.
- a. of OAS: agreed; however, there are specifics here that disallow these teachings on some processors



Items 27 to 41 discussions: 29

- did not understand this item

Items 27 to 41 discussions: 33

- our patent only addresses L3 pre-fetching
- we think this is not new matter

Items 27 to 41 discussions: 34

- could remove if Examiner Vicary (EV) is adamant

Items 27 to 41 discussions: 38

- we will say we decrease time but only at the cost of increasing effort
- with new more specific claims item 38 may become moot

Items 27 to 41 discussions: 39:41

- we agree with EV's comments

Items 42 to 46 discussions: 42:46

- we agree with EV's comments

Items 47 to 58 discussions: 48

- Gustavson only gives general guidelines
- the current invention is about new forms of algorithmic pre-fetching not covered in Gustavson
- these new forms apply recent new processors which did not exist at the time when Gustavson was published

Items 47 to 58 discussions: 49

- new claim 1. will be specific to the new forms of pre-fetching

Items 47 to 58 discussions: 50

- multiple loads of a special type need to be overcome
- the Gustavson paper does not discuss this aspect of the current invention
- new claim 1 will address how this new aspect can be handled

Items 47 to 58 discussions: 51:58

- see discussion of item 50

Items 59 to 63 discussions: 60

- new specific claims will address this objection
- see slides 5 to 9 of this presentation

Items 59 to 63 discussions: 61

- new claim(s) will address EV's objection

Items 59 to 63 discussions: 62

- new claim(s) will address EV's objection
- could not find Linear Algebra compiler references in the Gustavson references
- see pages 11 and 12 of the 6/19/07 amendment which are re-stated in slides 5 to 9 of this presentation

Items 59 to 63 discussions: 63

- lines 3 to 7 of item 7 will be incorporated into the new set of claims

Items 64 to 66 discussions: 64 m.

- the reason any conventional compiler cannot be a linear algebra (LA) compiler is that an array is not a matrix. this fact is not in the new Gustavson reference B.
- any claim about a LA compiler will not be obvious from reference B.
- reference B refers to L2 pre-fetching. this invention is about L3 pre-fetching